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Size Reduction of Wilkinson Power Divider using a Combination of Parallel Coupled Lines and Defective Microstrip Structures

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ABSTRACT This work describes a miniaturized power divider (PD) using the combination of two symmetrical parallel coupled lines (PCL) and a defective microstrip structure (DMS). The proposed PD is intended for 2.4 GHz wireless local area network (WLAN) applications. DMS structures are used to improve PD performance while also decreasing its size. Initially, to reduce the circuit size, quarter-wavelength lines were replaced with PCL's. It is observed that the size of PD is 0.42λgX0.53λg, representing a 25.3% decrease. Furthermore, four DMS structures are integrated into the design to reduce the overall size by 43% as compared with conventional Wilkinson PD at 2.4 GHz. The final size of PD is 0.35λgX0.47λg. Required equations are provided for the optimization of the DMS structure. The proposed PD has a return loss, isolation performance, and power division of around 16 dB, -15 dB, and -3.3 dB, respectively. The designed PD is fabricated on the substrate of Rogers RT/duroid 5880 with ε_r=2.2.

INDEX TERMS Defective Microstrip Structure (DMS), power divider (PD), Wireless Local Area Network (WLAN)

I. INTRODUCTION

THREE crucial aspects of the design of a microstrip power divider that affect the quality of the final product are harmonic suppression, size reduction, and introduction loss. Therefore, improving each of these factors leads to a more effective design. A method for improving performance and reducing the size of a Wilkinson power divider (WPD) is presented in this paper. Several microwave applications, such as antenna arrays, RF multipliers, mixers, and power amplifiers, make extensive use of power dividers (PD). In [1] Incorporating four high-low impedance resonators into the traditional PD reduces the PD size by as much as 36.5%. A low-impedance line cascades with a high-impedance line to form a high-low-impedance resonator. Because of their shorter electrical length, Quarter-wave-like transformers (QWLT) can replace traditional quarter-wave transformers (QWT), resulting in a reduction of up to 25% in PD size. In [2] To achieve PD size reduction, a periodic defective microstrip structure (DMS) pattern is added at the top of the microstrip line. In [3] Open stubs are utilized at each end of the transmission line in a WPD, and low-pass filters (LPFs) are introduced into each quarter-wavelength transmission line. A periodic DMS is put at the top of the microstrip line to lower the PD size. The authors replaced λ/4 transmission lines with multi-section π-structures to obtain miniaturization of UWB PD. The standard π-type configuration has a transmission line, two open stubs, and various electrical lengths and impedances [7,4]. 50% of PD size reduced in [5], two QW branches have been replaced with in place of the capacitors at the microstrip line's outside borders, two open-ended stubs were put inside the circuit loop. In [6], The defective microstrip structure (DMS) can minimize antenna size, adjust its performance, help in obtaining immunity to electromagnetic interference noise, and, because of its simple geometry, may be effortlessly integrated into the design structure. In [8] When the λ/4 transmission line is replaced, a tri-mode resonator is utilized as an alternative. Improvements in isolation were made possible by the implementation of a distributed stepped-impedance resonator network. An insertion loss of around 1.6 dB is associated with a substrate-integrated waveguide (SIW) power divider developed using a pair of open complementary split-ring resonators (OCSRRs) to reduce the size of the circuit [9]. In [10], to reduce harmonics, the standard PD has two tiny microstrip resonating cells that are laid out in a meandering pattern. These cells are inserted into quarter wavelength lines. Size reduction of more than 65%

compared to the traditional divider is achieved by the suggested PD. In [11], author made use of the traditional quarter-wavelength transmission lines have been substituted with a LPF.In [12], the author replaced λ/4 transmission lines with open and short-circuited stubs (OSCS), but the size of device is 50mmX50mm. In [13], Mukesh Kumar et al. proposed a Gysel power divider (GPD) with multiple coupled lines rather than a single line. This suppresses the second hormonic and simultaneously reduces the size of PD by 62%. In [14] The proposed PD is 55% smaller when rectangular and oval-shaped resonators are used instead of QWTLs. In [15] The size is reduced by replacing the QWTLs that make up the WPD with a matched pair of parallel transmission lines (PPTLs). When compared to a CWPD with a defective ground plane, this effectively reduces the WPD circuit size by 43%. The particle swarm optimization (PSO) technology is being used to minimize the size. In [16], two QW branches of the standard WPD are substituted by two LC branches. Each branch is made up of a small inductor, two TLs, and a series LC circuit. Fabrication is difficult due to the higher number of passive components. In [17] A meandering line is employed to realize PD, and an open shunt stub matching network is added to achieve a compact structure. For better performance, each arm has a vertical Periodic Defected Ground Structure (DGS) installed below it. In [18], B.Eppe et al. proposed an FPD with capacitive gap end coupled lines, operating at 2.4GHz, with the dimension of the FDP being 2.2 λgX0.27 λg. In [19], the author presents a miniaturized WPD capable of attenuating undesirable harmonics up to the 19th harmonic. An LPF was implanted as the typical WPD's QWTLs. The high impedance line is meandering to reduce the size of the intended design. To reduce the high frequency, a simple T-shaped resonator is added. In [20], the author developed a compact and simple PD that utilizes coupled lines to achieve a triple-band filtering response. The PD provided has a tri-band filtering response.

In this paper, a miniaturized WPD is designed and implemented. Initially, a WPD is designed at 2.75 GHz.It consists of two pairs of parallel coupled lines instead of one pair quarter wavelength lines. PCLs plays a significant role in achieving the required frequency operation, which is regulated only by the coupled line characteristics, with no extra components. With these PCLs the size of PD was reduced by 25.3%(0.42λgX0.53λg). Further, four square-shaped DMS structures are added on the top of PCLs that provide a size reduction of 43%(0.35λgX0.47λg) by means of shifting the frequency from 2.75 GHz to 2.4 GHz.

In DMS, adding slots in the microstrip feedline provides an alternative current path. Furthermore, this DMS structure modifies the inductance and capacitance of the input impedance, resulting in a variation in operating frequency. The operating center frequency of the PD varies by optimizing the dimensions of DMS applied to a microstrip line. The inserted DMS pattern has an equivalent additional capacitance and inductance that was size of the PD reduced, an analytic calculation approach is explained, and the resulting line impedance is used to design the PD. This work introduces a unique methodology for the miniaturization of power divider (PD) by adjusting the resonant frequency (f_0) through the use of DMS structures on microstrip lines while preserving the physical dimensions of the PD.

II. MINIATURIZATION OF PD

A. Design of Filtering Power Divider

In this work, initially a bandpass filter (BPF) is constructed using parallel coupled microstrip lines which is shown in Figure 1. Figure 2 illustrates the proposed filtering power divider (FPD), consisting of two identical PCL BPFs and a resistor functioning as an isolation network. The simulation results of the proposed FPD are shown in Figure 4. The resonance frequency of the FPD is 2.75 GHz.At this frequency, the reflection coefficient (S_{11}) and power divisions (S_{21}=S_{31}) are 11 dB, and 3.5 dB.

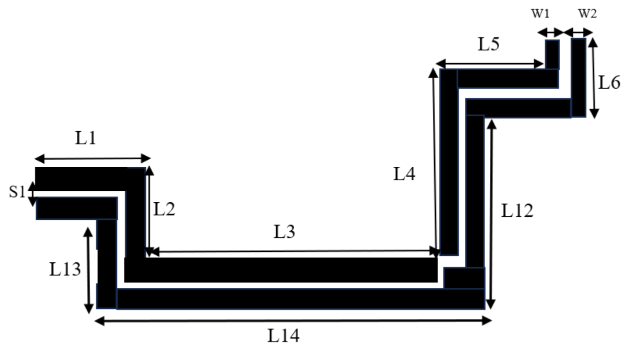


FIGURE 1. Schematic representation of BPF with coupled lines

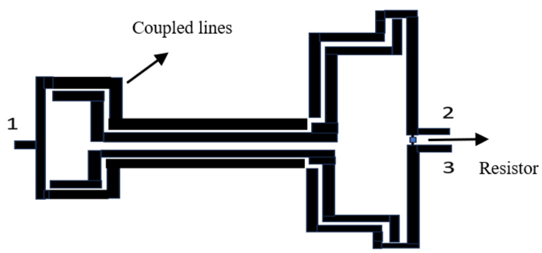


FIGURE 2. Schematic representation of PD

B. Design of Filtering Power Divider with DMS

To design the PD with a DMS pattern, it is necessary to provide the proper characteristic impedance of the DMS microstrip line. Accurately calculating the Zc is important for successfully applying DMS patterns to low- and high-frequency circuits and systems.

The square-shaped DMS is etched in the microstrip line of the PD, as depicted in Figure 3(a). The distribution density of current is influenced by both the path of the line and the presence of defected slots or discontinuities on the signal line.

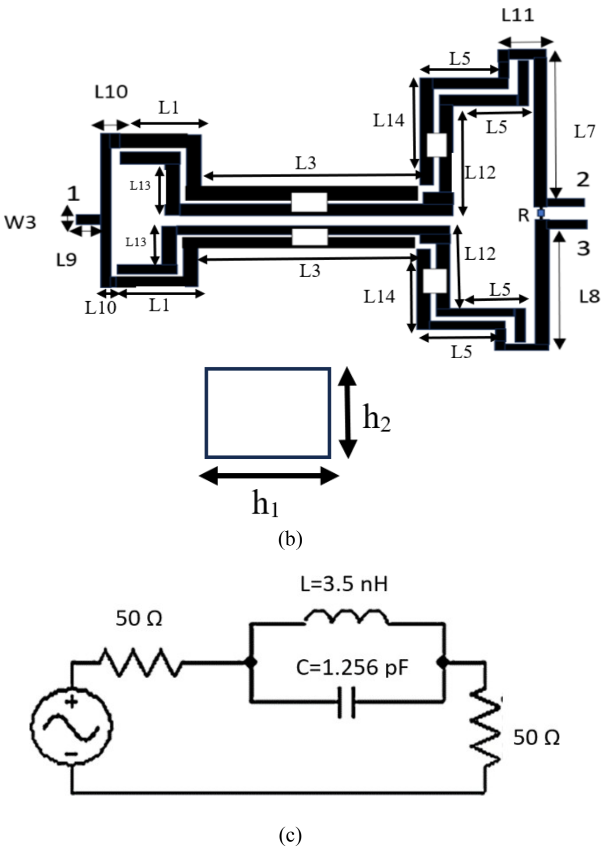


FIGURE 3. (a) Schematic representation of PD with DMS (b) Structure of DMS (c) Equivalent circuit of DMS

After that, the generated current distribution becomes recognized as a physical model. To examine the impact of DMS on the Z_c of a transmission line, we have considered DMS with specific dimensions i.e. length h_1 = 2 mm and width h_2 = 2 mm. The inclusion of the slot width (h_2) introduces a certain capacitance value. In contrast, the slot length (h_1) adds extra inductance to the normal 50Ω microstrip line, resulting in the development of slow wave characteristics. The structure of proposed DMS is shown in Figure 3(b). Square-shaped DMS (SSDMS) can be represented by an equivalent L-C circuit, as depicted in Figure 3(c).

The inductance L and capacitance C values can be calculated by using equations (1) & (2), these are 3.5 nH and 1.256 pF. The line impedance can be obtained by equation (3). The calculated line impedance Z_c is 50.2Ω with above L and C [6].

$$C = \frac{W_c}{2Z_0(W_0^2 - W_c^2)} \quad (1)$$

$$L = \frac{1}{4\pi^2 f_0^2 C} \quad (2)$$

$$Z_C = \sqrt{\frac{L}{C}} \quad (3)$$

$$S_{11} = 20\,log|r| \quad (4)$$

$$Z_{in} = Z_0 \frac{1+|r|}{1-|r|} \quad (5)$$

$$Z_{DMS} = \sqrt{Z_{in} Z_0} \quad (6)$$

Increasing the total size ($h = h_1+h_2$) of the DMS results in a corresponding increase in capacitance, which can be attributed to the improved total electrical path length (θ). This, in turn, enhances the slow-wave characteristics of the device. The relationship between total size and characteristic response variation is illustrated in Figure 5. Figure 5(a) depicts the shift of S_{11} with various h_1 values while keeping the h_2 constant at 2 mm. Figure 5(b) depicts the change in S_{11} with different h_2 values while maintaining the h_1 constant at 2 mm. Figure 5(c) presents the variations in S_{11} for different values of h_1 and h_2. All results in Figure 5 expressed a shift of S_{11} towards the lower frequency as the size h of the DMS varied. Additionally, Table 2 and Figure 6 present the changes in various parameters, including effective line impedance (Z_c), capacitance(C), and resonance frequency(f_0). Figure 6(a) shows the impact of DMS on frequency parameters. As the DMS size 'h' increases, the resonant frequency shifts to a lower frequency. According to the preceding results, if the value of h shifts from 3.2mm to 4mm, the value of S_{11} shifts from 2.64 GHz to 2.4 GHz. Figure 6(b) depicts the variation of Z_c with h, and it becomes evident that line impedance decreases as the size of DMS increases. These line impedance values are obtained by substituting the equations (1) and (2) in equation (3). If a DMS is placed on the microstrip line the current distribution is interrupted and the electrical path length increases. Thus, the effective inductance and capacitance values vary appropriately. Figure 6(c) depicts the variation of capacitance with the dimensions of DMS. The value of capacitance increase with 'h' from 1.038 pF to 1.256 pF. These capacitance values are obtained from equation (1).

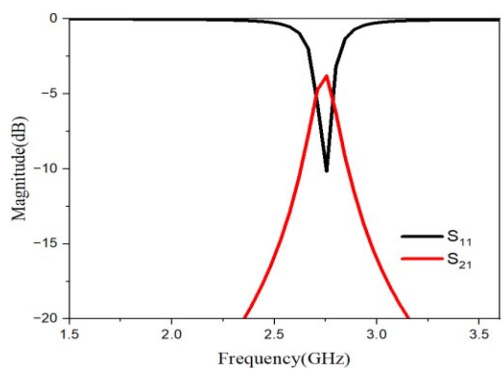
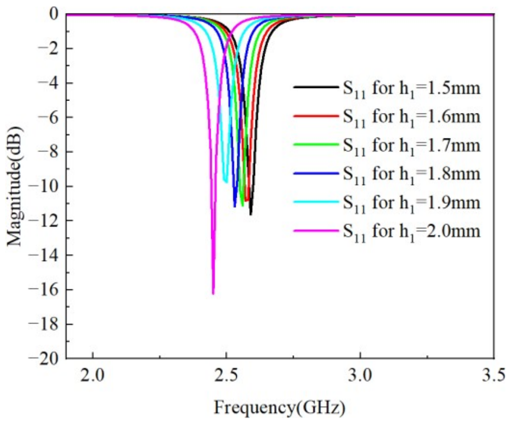


FIGURE 4. Simulated results of FPD



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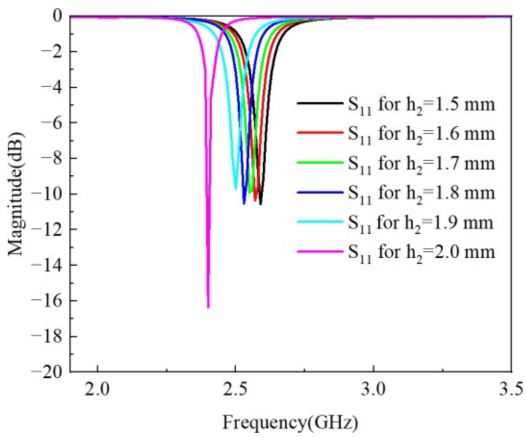

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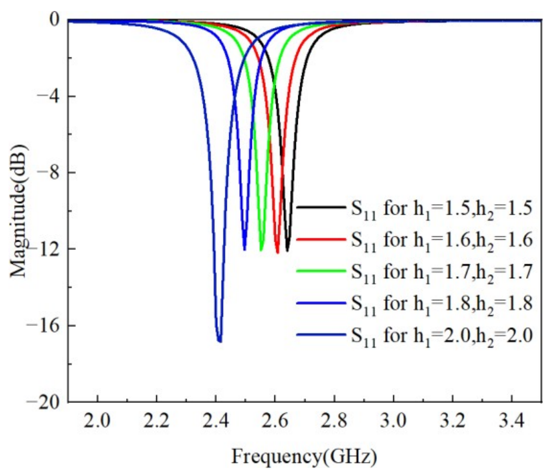

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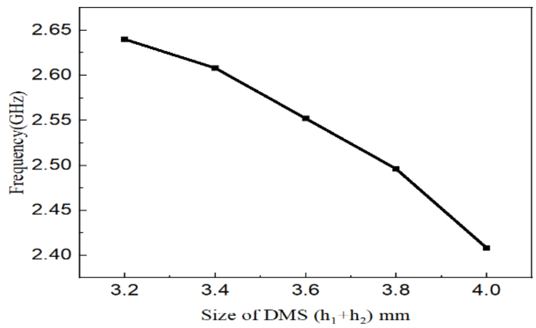
FIGURE 5. Effect of DMS on PD (a) h2=2mm and h1 varied (b) h1=2mm and h2 varied (c) Both h1&h2 varied

TABLE I. DESIGNED PARAMETERS OF PD(MM)

L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}	L_{12}
4	4	10.9	12.2	5	4	15.71	15.71	3	1.9	5.56	12.3
L_{13}	L_{14}	h_1	h_2	W_1	W_2	W_3	S_1	Size(λgXλg)			
4	15.6	2.2	1.8	1	1	1.56	0.3	0.35x0.47			



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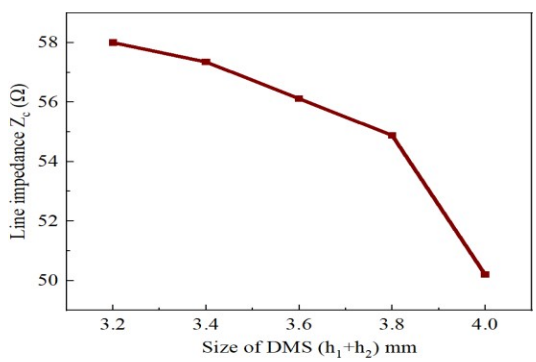

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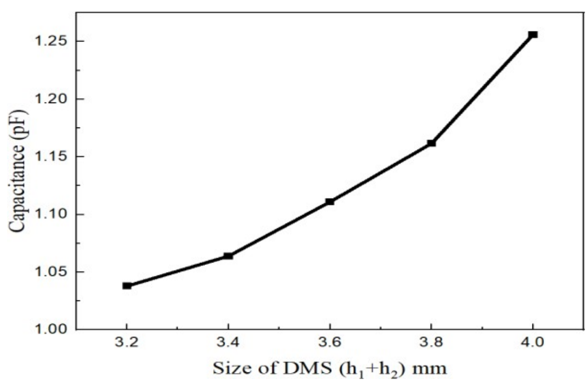


(c)

FIGURE 6. DMS with different parameters (a) variation of S_{11} (b) variation of Line impedance (Zc) (c) variation of capacitance(C)

When the resonance occurs, the reflection coefficient (Γ) is greatest when the electrical length (θ) of the line with DMS is π/2, and it may be determined from S_{11} using equation (4). Equation (5) can be used to calculate Z_{in} after |Γ| is known. In the end, using equation (6), we can determine the impedance of the microstrip line that contains DMS. The proposed PD design parameters are shown in Table 1.

The input power, which is applied at port 1, is splitted between two output ports, port 2 and port 3, with each port receiving a power value of 3 dB. Figure 7 shows a picture of the designed PD simulation results. The responses above show that the suggested structure operates at 2.4 GHz, and gives a power division of 3 dB or equal. The developed PD performance has been evaluated using HFSS EM Simulation software.

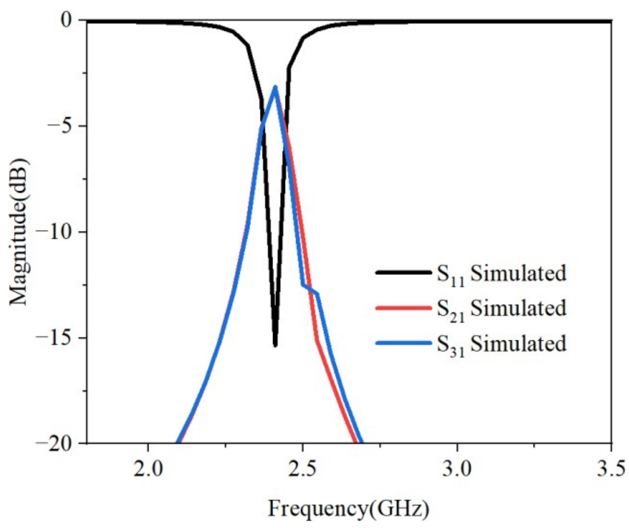
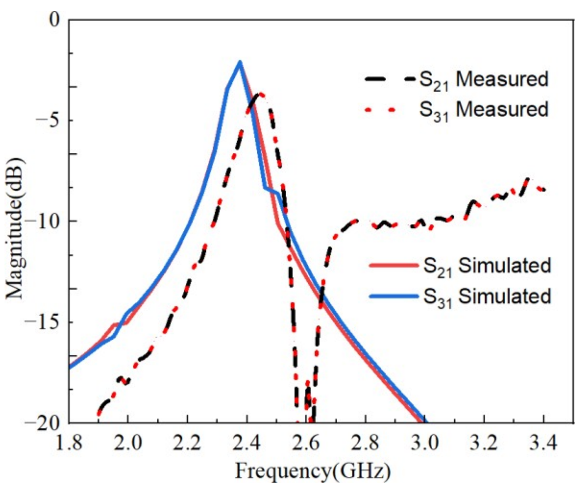


FIGURE 7. Simulated results of PD with DMS



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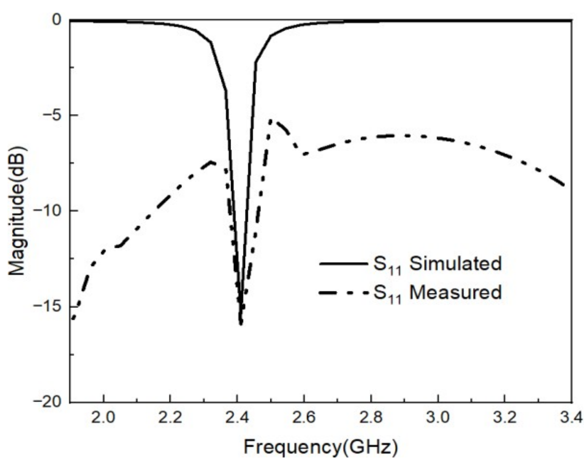

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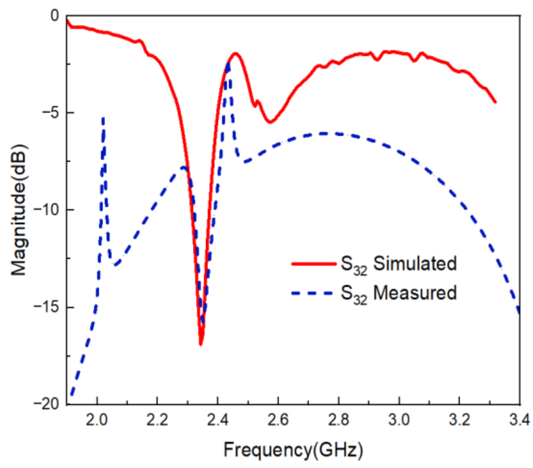
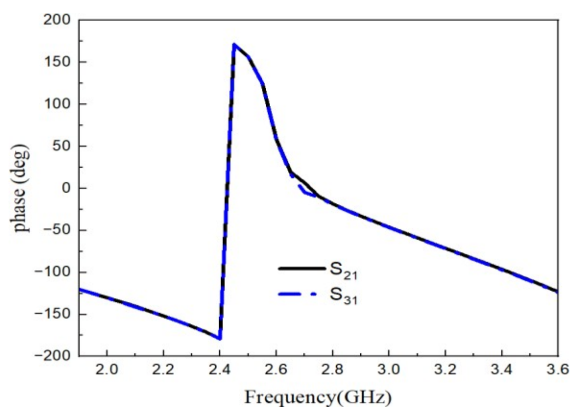


(c)

FIGURE 8. Comparison of Measured and Simulated results of designed PD (a) Power division of PD (S12) (b) Reflection coefficient (S11) (c) Isolation (S23)

TABLE 2. DMS size verses various parameters

h(mm)	Frequency(GHz)	$Z_c(\Omega)$	C(pF)
3.2	2.64	58	1.038
3.4	2.608	57.35	1.064
3.6	2.552	56.12	1.111
3.8	2.496	54.88	1.1616
4	2.408	50.2	1.256



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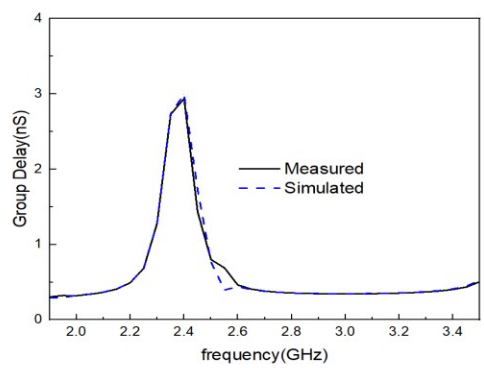

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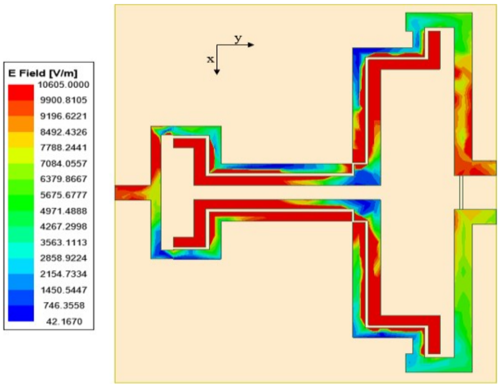

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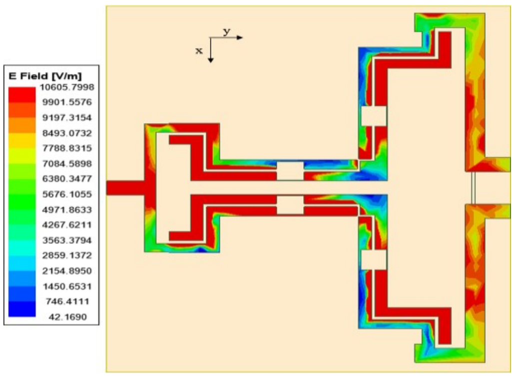

(d)

FIGURE 9. (a) phase relation (b) Group Depay of designed PD (c) Surface current distribution of designed PD without DMS (d) Surface current distribution of designed PD with DMS

III. RESULTS AND DISCUSSIONS OF POWER DIVIDER

The proposed PD is constructed using an RT/Duroid (ε_r=2.2), 0.508mm thick substrate, using microstrip line. The suggested PD has been developed, built, and measured. The developed PD performance has been evaluated using HFSS software, which compares it to simulation findings. The measurement setup for the designed PD model is depicted in Figure 11. Figure 10 shows pictures of the intended construction. Figures 8 provide a comparison of the measured and simulated results. At the operational frequency, the measured results of intended PD had a return loss S_{11}=16 dB and isolation S_{23}=15 dB, and an insertion loss of 3.1 ± 0.2 dB at the output ports. The simulated results of the designed pd include return loss S_{11}=18 dB, isolation S_{23}=16 dB, and an insertion loss of 3.1 dB at the output ports. There is a good match between the simulated and measured outcomes. The dimensions of PD are 0.35λg x 0.47λg. The surface current of the designed PD is depicted in Figure 9(c) and 9(d). Figure 9(c) shows the current distribution of PD without DGS and Figure 9(d) represents the current distribution of PD with DGS. The PD design has a group delay of around 3ns due to the incorporation of DMS on the microstrip lines, which disturbs the surface current flow between port 1 andport 2.9(a) depicts the good phase relation between ports 1 and 2. Figure 9(b) displays the group delay of the designed PD from the input port to the output port.

The suggested design offers sufficient power division and isolation. The size of the proposed PD is 43% less than the CWPD.Table.3 compares the proposed filtering power divider's performance to previously reported designs. The insertion loss of the proposed PD is only 3.3 dB, Compared to References [7], [8], [11], [12]. The designed PD is suitable for WLAN applications, and the design is also simple.

TABLE 3. Comparison of proposed PD with other works.

Ref.	Frequency (GHz)	Insertion loss(dB)	Method	Size reduced (%)	Size (λgXλg)
[7]	2.15	1.3	Resonators, Isolation network	--	0.59x0.29
[8]	5.68	1.6	OCSRRs	25	0.31x0.14
[11]	0.9	0.17	Open and short stubs	---	0.13x0.2
[12]	1.0	0.22	Coupled line section	62	0.32x0.16
[15]	2.4	0.1	LC branches	57	--------
Here	2.4	0.2	PCL and DMS	43.1	0.35x0.47

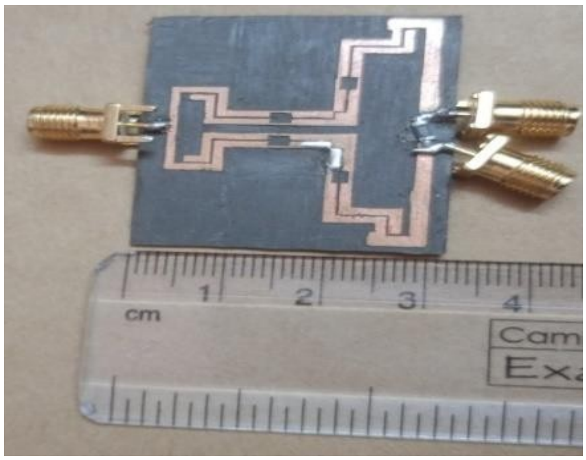

FIGURE 10. Photograph of the developed PD

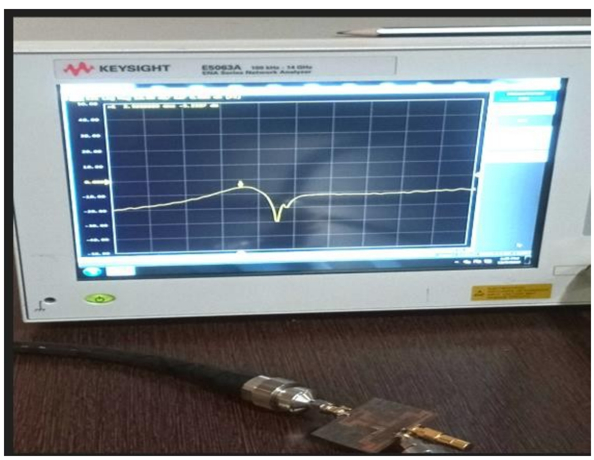

FIGURE 11. Measurement setup of the designed PD

IV. CONCLUSION

An enhanced design based on DMS-loaded parallel coupled transmission lines demonstrates a reduced WPD for various microwave applications. The overall size reduction is 43% at the resonant frequency of 2.4 GHz. The determined insertion loss is 3.3 dB, reflection coefficient (S_{11}) and isolation (S_{23}) performance are better than -15 dB at the operating frequency, and a comparison of state-of-the-art devices in the literature demonstrates that the designed structure provides an excellent trade-off between size and performance. The proposed PD design uses a planner printed circuit board with a smaller circuit size, which is in high demand in microwave wireless communication systems like WLAN, Cognitive radio, Antenna feed systems etc.

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